In the Claims

1. (currently amended) A method of creating a photomask layout for projecting an image of an integrated circuit design comprising:

creating a layout of spaced integrated circuit shapes to be projected via ~~the~~ a photomask;

creating Voronoi cells around the spaced integrated circuit shapes;

determining bisectors between adjacent ones of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant from edges of the adjacent spaced integrated circuit shapes and defining shared boundaries of adjacent Voronoi cells;

identifying different types of bisectors based on ~~the~~ vertices thereof consisting of a first type of bisector, a second type of bisector, and a third type of bisector; ~~and~~

creating sub-resolution assist features between the adjacent ones of the spaced integrated circuit shapes based on the different types of bisectors, whereby,

if any of the identified bisectors are of said ~~a~~ first type of bisector~~bisectors~~, the sub-resolution assist features extend along the first type of bisector ~~bisectors~~ to a first vertex of said bisector ~~their respective bisectors~~ and extend beyond ~~the~~ a second vertex of said bisector~~bisectors~~,

if any of the identified bisectors are of saida second type of bisectorbisectors, the sub-resolution assist features extend along the second type of bisector bisectors with ends terminating on and equidistant away from vertices of said second type of bisectorbisectors,

if any of the identified bisectors are of saida third type of bisectorbisectors, at least a pair of sub-resolution assist features are positioned on opposing sides of their respective bisector, each between one of the adjacent shape edges and said bisector, whereby upper ends of each of said pair of sub-resolution assist features terminates a distance beyond the ends of their respective adjacent shape edges;

generating a pattern on the photomask corresponding to said photomask layout; and

projecting said photomask layout via said photomask onto a resist layer.

2. (cancelled)

3. (original) The method of claim 1 wherein the adjacent ones of the spaced integrated circuit shapes are parallel to each other and the sub-resolution assist features along the bisectors are parallel to the spaced integrated circuit shapes.

4. (previously presented) The method of claim 1 further including prioritizing creation of the sub-resolution assist features in accordance with the different types of bisectors.

5. (original) The method of claim 1 further including extending at least some of the sub-resolution assist features beyond the bisectors on which they are created.

6. (original) The method of claim 1 further including extending at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features.

7. (original) The method of claim 1 further including removing at least one of the sub-resolution assist features along the bisectors prior to finalizing the photomask layout.

8. (original) The method of claim 1 wherein the integrated circuit shapes are two-dimensional and include shapes having edges parallel and perpendicular to each other, between which the bisectors are located.

9. (original) The method of claim 1 wherein the integrated circuit shapes are two-dimensional and include shapes having lengths of parallel edges in which an edge of one shape ends at a point within the length of the other shape, between which the bisectors are located.

10. (currently amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for creating a photomask layout for projecting an image of an integrated circuit design, said method steps comprising:

creating a layout of spaced integrated circuit shapes to be projected via ~~the~~ a photomask;

creating Voronoi cells around the spaced integrated circuit shapes;

determining bisectors between adjacent ones of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant from edges of the adjacent spaced integrated circuit shapes and defining shared boundaries of adjacent Voronoi cells;

identifying different types of bisectors based on ~~the~~ vertices thereof consisting of a first type of bisector, a second type of bisector, and a third type of bisector; ~~and~~

creating sub-resolution assist features between the adjacent ones of the spaced integrated circuit shapes based on the different types of bisectors, whereby,

if any of the identified bisectors are of ~~said~~a first type of bisector~~bisectors~~, the sub-resolution assist features extend along the first type of bisector ~~bisectors~~ to a first vertex of said bisector ~~their respective bisectors~~ and extend beyond ~~the~~ a second vertex of said bisector~~bisectors~~,

if any of the identified bisectors are of said ~~a~~ second type of bisector~~bisectors~~, the sub-resolution assist features extend along the second type of bisector ~~bisectors~~ with ends terminating on and

equidistant away from vertices of said second type of bisectorbisectors,

if any of the identified bisectors are of said a third type of bisectorbisectors, at least a pair of sub-resolution assist features are positioned on opposing sides of their respective bisector, each between one of the adjacent shape edges and said bisector, whereby upper ends of each of said pair of sub-resolution assist features terminates a distance beyond the ends of their respective adjacent shape edges.

11. (cancelled)

12. (original) The program storage device of claim 10 wherein, in the method, the adjacent ones of the spaced integrated circuit shapes are parallel to each other and the sub-resolution assist features along the bisectors are parallel to the spaced integrated circuit shapes.

13. (previously presented) The program storage device of claim 10 further including, in the method, prioritizing creation of the sub-resolution assist features in accordance with the different types of bisectors.

14. (original) The program storage device of claim 10 further including, in the method, extending at least some of the sub-resolution assist features beyond the bisectors on which they are created.

15. (original) The program storage device of claim 10 further including, in the method, extending at least some of the sub-resolution assist features beyond the bisectors on which they are created to connect to other sub-resolution assist features.

16. (currently amended) An article of manufacture comprising a ~~computer-usable~~ computer readable medium having computer readable program code means embodied therein for creating a photomask layout for projecting an image of an integrated circuit design, the computer readable program code means in said article of manufacture comprising:

computer readable program code means for creating a layout of spaced integrated circuit shapes to be projected via ~~the~~ a photomask;

computer readable program code means for creating Voronoi cells around the spaced integrated circuit shapes;

computer readable program code means for determining bisectors between adjacent ones of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant from edges of the adjacent spaced integrated circuit shapes and defining shared boundaries of adjacent Voronoi cells;

computer readable program code means for identifying different types of bisectors based on ~~the~~ vertices thereof consisting of a first type of bisector, a second type of bisector, and a third type of bisector; ~~and~~

computer readable program code means for creating sub-resolution assist features between the adjacent ones of the spaced integrated circuit shapes based on the different types of bisectors, whereby,

if any of the identified bisectors are of saida first type of bisectorbisectors, the sub-resolution assist features extend along the first type of bisector bisectors to a first vertex of said bisector their respective bisectors and extend beyond the a second vertex of said bisectorbisectors,

if any of the identified bisectors are of said a second type of bisectorbisectors, the sub-resolution assist features extend along the second type of bisector bisectors with ends terminating on and equidistant away from vertices of said second type of bisectorbisectors,

if any of the identified bisectors are of said a third type of bisectorbisectors, at least a pair of sub-resolution assist features are positioned on opposing sides of their respective bisector, each between one of the adjacent shape edges and said bisector, whereby upper ends of each of said pair of sub-resolution assist features terminates a distance beyond the ends of their respective adjacent shape edges.

17. (cancelled)

18. (original) The article of manufacture of claim 16 wherein the adjacent ones of the spaced integrated circuit shapes are parallel to each other and the sub-resolution assist features along the bisectors are parallel to the spaced integrated circuit shapes.

19. (previously presented) The article of manufacture of claim 16 wherein the computer readable program code means in said article of manufacture further includes computer readable program code means for prioritizing creation of the sub-resolution assist features in accordance with the different types of bisectors.

20. (original) The article of manufacture of claim 16 wherein the computer readable program code means in said article of manufacture further includes computer readable program code means for extending at least some of the sub-resolution assist features beyond the bisectors on which they are created.

21. (previously presented) The method of claim 1 wherein each of the first type of bisectors has a vertex thereof between three adjacent shape edges, and each of the second and third types of bisectors have a vertex thereof between an adjacent shape edge and an adjacent shape corner.

22. (previously presented) The method of claim 21 wherein in the step of identifying the different types of bisectors,

if a distance between edges of adjacent shapes is less than a predetermined maximum edge distance, then the bisectors are of the first or second type of bisectors, and

if the distance between edges of adjacent shapes is greater than said predetermined maximum edge distance then the bisectors are of the third type of bisectors.

23. (previously presented) The method of claim 1 wherein in the third type of bisectors, further including at least a third sub-resolution assist feature positioned between the pair of sub-resolution assist features.

24. (previously presented) The method of claim 1 further including determining whether each sub-resolution assist feature is extendable, whereby,

if the sub-resolution assist feature is extendable, then extending the sub-resolution assist feature, and

if the sub-resolution assist feature is non-extendable, then deleting the sub-resolution assist feature.

25. (currently amended) A method of creating a photomask layout for projecting an image of an integrated circuit design comprising:

creating a layout of spaced integrated circuit shapes to be projected via ~~the~~ a photomask;

creating Voronoi cells around the spaced integrated circuit shapes;

determining bisectors between adjacent ones of the spaced integrated circuit shapes, the bisectors comprising locus of points equidistant from edges of the adjacent spaced integrated circuit shapes and defining shared boundaries of adjacent Voronoi cells;

identifying different types of bisectors based on vertices thereof; and

creating sub-resolution assist features based on said different types of bisectors along at least some of the bisectors between the adjacent ones of the spaced integrated circuit shapes, the sub-resolution assist features extending along the bisectors beyond an adjacent spaced integrated circuit shape, whereby each sub-resolution assist feature has a length at least five times its width, such that, those that violate this rule are deleted.